AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS

1. (Original) A data processor comprising n-bit instructions and 2n-bit instructions in an instruction set and including an instruction control unit that can decide whether registers specified in register specification fields of the instructions conflict between the instructions,

wherein the 2n-bit instructions including register specification fields include the register specification fields in the first half n bits thereof, and

wherein the register specification fields in the first half n bits have the same placement as register specification fields in the n-bit instructions.

2. (Original) A data processor comprising n-bit instructions and 2n-bit instructions in an instruction set and including an instruction control unit that can decide whether registers specified in register specification

fields of the instructions conflict between the instructions,

wherein the 2n-bit instructions including register specification fields include the register specification fields in one of the first half n bits or latter half n bits thereof, and

wherein the register specification fields in the first half n bits or latter half n bits include the same placement as register specification fields in the n-bit instructions.

3. (Original) The data processor according to claim 2,

wherein the instruction set comprises instructions in which register specification fields aligned with the register specification fields in the n-bit instructions are placed in the first half n bits of the 2n-bit instructions, and

wherein the instruction set further comprises instructions in which register specification fields aligned with the register specification fields in the n-bit instructions are placed in the latter half n bits of the 2n-bit instructions.

4. (Original) The data processor according to claim 1,

wherein n bits are 16 bits, and 2n bits are 32 bits.

5. (Original) The data processor according to claim 1,

wherein the instruction control unit, in response to register conflict, is able to perform control such as the stalling of pipeline stages or the forwarding of operation data write to general purpose registers.

6. (Original) The data processor according to claim 1,

wherein the data processor is able to execute instructions in single scalar mode.

7. (Currently amended) The data processor according to ~~one of claims~~claim 1 ~~to 3~~,

wherein the data processor can execute instructions in superscalar mode.

8. (Original) The data processor according to claim 2,

wherein the instruction control unit, in response to register conflict, is able to perform control such as the stalling of pipeline stages or the forwarding of operation data write to general purpose registers.

9. (Original) A data processor comprising first n-bit instructions and second 2n-bit instructions each including register specification fields in an instruction set,

wherein the second instructions are instructions with an immediate value or displacement value extended to the first instructions,

wherein the second instructions include register specification fields in the first half n bits thereof, and

wherein the register specification fields in the first half n bits of the second instruction comprises the same placement as the register specification fields in the first instructions.

10. (Currently amended) The data processor according to claim 9,

wherein the data processor includes third n-bit instructions including register specification fields,

wherein the third instructions and the second instructions are different from each other in the number of operands specifiable in the register specification fields, and ~~and~~

wherein register specification fields of the third instructions and those of the second instructions are aligned in the start of the register specification fields with respect to the start of the first instructions.

11. (Original) A data processor comprising first n-bit instructions and second 2n-bit instructions each including register specification fields in an instruction set,

wherein the second instructions include register specification fields in one of the first half n bits and the latter half n bits thereof, and

wherein the placement of the register specification fields in the first half n bits or the latter half n bits

is the same as the placement of the register specification fields in the first instructions.

12. (Original) The data processor according to claim 11,

wherein the data processor includes third n-bit instructions including register specification fields,

wherein the third instructions and the second instructions are different from each other in the number of operands specifiable in the register specification fields, and

wherein register specification fields of the third instructions and those of the second instructions are aligned in the start of the register specification fields with respect to the start of the first instructions.

13. (New) The data processor according to Claim 2,

wherein the data processor can execute instructions in superscalar mode.

14. (New) The data processor according to claim 3,

wherein the data processor can execute instructions in superscalar mode.